

IN THE CLAIMS

Claim 1 (original): A semiconductor component, comprising:
a substrate having a major surface;
a trench having first and second sidewalls extending from the major surface into the substrate;
a first column of memory cells adjacent the first sidewall; and
a trench line disposed in the trench, wherein the trench line is electrically coupled to the first column of memory cells.

Claim 2 (original): The semiconductor component of claim 1, wherein the first column of memory cells comprises at least one memory cell having a gate structure, a drain region, and a source region.

Claim 3 (original): The semiconductor component of claim 2, further including a first connector, wherein the first connector electrically couples one of the source region or the drain region to the trench line.

Claim 4 (original): The semiconductor component of claim 3, further including a second connector, wherein the second connector electrically couples the other of the source region or the drain region to the trench line.

Claim 5 (original): The semiconductor component of claim 3, wherein the trench line serves as a bit line.

Claim 6 (original): The semiconductor component of claim 2, further including a drain connector, wherein the drain connector electrically couples the drain region of the at least one memory cell to the trench line.

Claim 7 (original): The semiconductor component of claim 6, further including a source connector, wherein the source connector electrically couples the source region of the at least one memory cell to the trench line.

Claim 8 (original): The semiconductor component of claim 2, further including a source connector, wherein the source connector electrically couples the source region of the at least one memory cell to the trench line.

Claim 9 (original): The semiconductor component of claim 8, further including a second column of memory cells, wherein the second column of memory cells is adjacent the second sidewall and comprises at least one memory cell having a gate structure, a drain region, and a source region.

Claim 10 (original): The semiconductor component of claim 8, further including another drain connector, wherein the another drain connector electrically couples the drain region of the at least one memory cell of the second column of memory cells to the trench line.

Claim 11 (original): The semiconductor component of claim 8, further including another source connector, wherein the another source connector electrically couples the drain region of the at least one memory cell of the second column of memory cells to the trench line.

Claim 12 (original): The semiconductor component of claim 1, further including a second column of memory cells, wherein the second column of memory cells is adjacent the second sidewall and comprises at least one memory cell having a gate structure, a drain region, and a source region.

Claim 13 (original): A memory device, comprising:

- a first memory cell having a gate structure, a drain region, and a source region;
- a second memory cell having a gate structure, a drain region, and a source region,

wherein the source region of the second memory cell is coupled to the source region of the first

memory cell, and wherein the first and second memory cells cooperate to form a first column of memory cells; and

a first trench line adjacent the first column of memory cells, wherein the source regions of the first and second memory cells are coupled to the first trench line.

Claim 14 (original): The memory device of claim 13, further including a second trench line adjacent the first column of memory cells, wherein the drain regions of the first and second memory cells are coupled to the second trench line.

Claim 15 (original): The memory device of claim 14, further including:

a third memory cell having a gate structure, a drain region, and a source region; and
a fourth memory cell having a gate structure, a drain region, and a source region, wherein the source region of the fourth memory cell is coupled to the source region of the third memory cell and the source regions of the third and fourth memory cells are coupled to the second trench line, and wherein the third and fourth memory cells cooperate to form a second column of memory cells.

Claim 16 (original): The memory device of claim 15, wherein the second trench line is between the first and second columns of memory cells.

Claim 17 (original): The memory device of claim 15, further including a third trench line adjacent the second column of memory cells.

Claim 18 (original): The memory device of claim 17, wherein the drain regions of the third and fourth memory cells are coupled to the third trench line.

Claim 19 (original): The memory device of claim 18, wherein the first trench line serves as a first bit line, the second trench line serves as a second bit line, and the third trench line serves as a third bit line.

Claim 20 (original): The memory device of claim 15, further including a first bit line coupled to the drain regions of the first and second memory cells.

Claim 21 (original): The memory device of claim 20, further including a second bit line coupled to the drain regions of the second and third memory cells.

Claim 22 (original): The memory device of claim 13, further including a first bit line coupled to the drain regions of the first and second memory cells.

Claims 23-31 (canceled)